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10/783,025	02/23/2004	Hitoshi Suwa	60188-781	3766

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EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,025	SUWA ET AL.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *5-13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 September 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02232004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Restriction Requirement

The Response to Restriction Requirement submitted on Jul 26, 2005 elected Species I, claims 1-4. Therefore, this action will assume that claims 5-13 have been withdrawn from consideration.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: "CS1" is not shown in Fig. 1, although it is described on page 10, line 17. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the examiner does not accept the changes, the applicants will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are also objected to because the connection between VIN and the drain of transistor M21 is missing from Fig. 4; and page 18, lines 2-3 identifies M31 of Fig. 6 as a charge

transfer transistor, but it appears to be shown as a capacitor since its drain and source are coupled together. It is suggested that drain-source connection be deleted so M31 is represented in the same manner as corresponding transistors M32 and M3n. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the examiner does not accept the changes, the applicants will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities: Page 11, line 10 "VI" should be --VIN-- to correspond to Fig 1. Page 15, line 15 "four" should be --fourth--. Line 10 of the amended paragraph for page 22 of the disclosure (shown on page 2 of the Preliminary Amendment submitted on Sep 21, 2004) should have "41 through 43" replaced with

--M41 through M43-- to be consistent with the other reference designators. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-4 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention.

Claim 1 recites the limitation "the control signal" in line 11. There is insufficient antecedent basis for this limitation in the claim. For example, how does this signal relate to either the "detection signal" or the "clock signal" already recited? Claims 2-4 carry over the rejection from claim 1.

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

In so far as being understood, claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pan. Fig. 4 of Pan shows booster circuit 400 comprising boosting section 410-430 including a plurality of serially-connected boosting cells 410-430 for boosting input voltage V0 in response to clock signal CLK from current control circuit 450 (e.g. see Fig 7), and outputting boosted voltage Vn; boosted voltage detector 460 for detecting boosted voltage Vn, and outputting a detection signal to current control circuit 450, wherein 450 can be considered one type of clock generator for outputting clock signal CLK in response to the detection signal. Fig. 6 shows an example of boosting cell 430, which comprises diode 670, and a plurality of boosting capacitors C1-Cn connected in parallel (e.g. see column 5, lines 1-4). Since Pan discloses voltage detector 460 sends a signal, and disables one capacitor when a predetermined voltage is reached (e.g. see column 4, lines 36-41, and column 5, lines 33-34). Therefore, one of ordinary skill in the art would understand this would also relate to when the detected boosted voltage is lower than, or equal to, a given voltage value. Since both Figs. 7 and 9 show current control circuit 450 providing clock signal CLK, which is understood to be one type of control signal, one of ordinary skill in the art would conclude that clock/control signal CLK is based on the detection signal output from boosted voltage detector 460 (e.g. see Fig. 6). Boosting cell 430 (shown in Fig. 6) of the boosting section also includes connection switching circuit (e.g. driving circuits) 610-630, wherein Figs. 7 and 9 show examples that can be used for Pan's driver circuits 610-630 (e.g. see column 5, lines 38-42, and column 6, lines 10-13). Whenever the pull-up, or pull-down, sections of at least two connection switching circuits are activated at the same time,

their corresponding capacitor will be connected in parallel with respect to each other. For example, if pull-down section T4 (see Fig. 7) of circuit 610 is turned on, and pull-down section T9 (see Fig. 9) of circuit 620 is turned on, their corresponding capacitors C1 and C2 are coupled in parallel between Vn and ground. However, Pan does not show a charge transfer transistor within each boosting cell. It would have been obvious to one of ordinary skill in the art to replace diode 670, within each boosting cell (e.g. see 430 in Fig. 6), with a corresponding diode-connected MOS transistor. This transistor will be a charge transfer transistor (e.g. it will allow charge transfer in only one direction), and claim 1 is rendered obvious. A MOS transistor is easy to fabricate, and would correspond to the use of MOS transistors within the driver circuits (e.g. see Figs. 7 and 9), thus ensuring the components would have similar operational characteristics (e.g. with respect to temperature or voltage).

In so far as being understood, claims 1-2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cave et al. (Cave), in view of Chang et al. (Chang). Cave et al. clearly shows a booster circuit in Fig. 2 comprising boosting section 12 with a plurality of boosting capacitors connected in parallel; boosted voltage detector 16 for detecting boosted voltage OUTPUT 14, and for outputting detection signal 66-70; and clock generator 26-28 (or the inherent circuitry that provides signals CLK 20,/CLK 20'). The boosting section also comprises connection switching circuit 42-46 for switching connections of capacitors 36-40 based on control signal 78 from control section 18, which is controlled by detection signal 66-70 from boosted voltage detector 16. However, the clock generator is neither clearly shown nor disclosed as outputting the clock signal in response to the detection signal from the boosted voltage detector. Chang shows/discloses a booster circuit in Fig. 1 having clock generator 106 outputting a clock signal

(not labeled) in response to the detection signal (not labeled) from regulator 110. Chang also discloses the control of the amplitude and frequency of the clock signal can be used to provide a stable output voltage with little or no ripple, adjust output current drivability, and consume less power (e.g. see column 3, lines 17-20, 25-30, and 44-45). Therefore, it would have been obvious to one of ordinary skill in the art to apply the teachings of Chang to Cave's circuitry. For example, Chang's regulator system 112 comprises boosted voltage detector 110 that could output a detection signal in response to detecting boosted voltage OUTPUT 14 of Cave, and that detection signal would be used to control clock generator 106 of Chang, which would provide the clock signal (e.g. CLK 20, /CLK 20') to control Cave's boosting section. Therefore, claim 1 is rendered obvious. By applying Chang's teachings to Cave's booster circuit, the modified booster circuit would have less output ripple, consume less current, and therefore be more efficient. Deeming Cave's control/sensing circuits 18/16 as a boosted voltage detection control section for outputting control signal 78, and Chang's regulator 110 as the boosted voltage detector for outputting the detection signal controlling clock generator 106, claim 2 is rendered obvious.

In so far as being understood, claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ogura, in view of Chang et al. (Chang). Ogura shows booster circuit VCa in Fig. 1, wherein VCa comprises boosting sections SGc/SGd (e.g. see Figs. 3-4, and related Fig. 2). The boosting section shown within each of Figs. 3 and 4 clearly shows a plurality of boosting capacitors that are connected in parallel with respect to their corresponding connection switching circuit (e.g. SW1a-SW1c of Fig. 3; and SW2a-SW2C in Fig. 4), wherein the switching connections are based on control signals S1a-S3a (e.g. see Figs. 1 and 7). These control signals

are determined from the detection of power supply voltage Vcc by boosted voltage detection control section DE1 (e.g. see column 18, lines 19-27), which provides them to the connection switching circuit. [Note: Although signal BE is only disclosed as a boost enable signal, it is understood signal BVBE depends on it, and for Ogura's boosting section VCa to operate properly, BVBE must be periodic (e.g. have alternating values). Therefore, it is believed that signal BE is some form of clocking signal, and not just a simple enable signal that has its logic level reversed on a one time basis just to enable the circuit. For example, if signal BE was set to remain at one logic level, signal BVBE would remain at a corresponding logic level. Without any periodic type signals, Ogura's boosting section VCa could not output a boosted voltage. Using Ogura's Fig. 3 as an example, if BVBE is always high, transistors N31, N32, and P33 would be on, thus connecting the capacitor(s) between Vcc and ground, and allowing them to charge. Unless BVBE changes logic levels, output Voutc of Fig. 3 would remain at Vcc, with no boosting action performed. The actual boosting action is performed after the charging operation, and when transistors N31, N32, and P3 are turned off, and transistors P31 and P32 are turned on. This configuration allows output voltage Voutc to become the sum of voltage Vcc (through P31) and the charged voltage across the capacitor(s), Therefore, for Ogura's circuit to operate, it would be understood boosting section VCa, and its boosting cells, must receive some type of periodic, or alternating, clocking signals.] However, Ogura does not show a clock generator outputting a clock signal, in response to a detection signal from a boosted voltage detector. Chang shows/discloses a booster circuit in Fig. 1 having clock generator 106 outputting a clock signal (not labeled) in response to the detection signal (not labeled) from regulator 110. Chang also discloses the control of the amplitude and frequency of the clock signal can be used to

provide a stable output voltage with little or no ripple, adjust output current drivability, and consume less power (e.g. see column 3, lines 17-20, 25-30, and 44-45). Therefore, it would have been obvious to one of ordinary skill in the art to apply the teachings of Chang to Ogura's circuitry. For example, Chang's regulator system 112 comprises boosted voltage detector 110 that would output a detection signal in response to detecting boosted voltage VB of Ogura, and that detection signal would be used to control clock generator 106 of Chang, which would provide clock signal BE that effectively controls Ogura's boosting section. Therefore, claim 1 is rendered obvious. By applying Chang's teachings to Ogura's booster circuit, the modified booster circuit would have less output ripple, consume less current, and therefore be more efficient. Deeming Ogura's block DE1 as a boosted voltage detection control section for outputting control signal S1a-S3a, and Chang's regulator 110 as the boosted voltage detector for outputting the detection signal controlling clock generator 106, claim 4 is rendered obvious.

No claim is allowable as presently written.

Allowable Subject Matter

However, claim 3 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure the booster circuit also comprises a power supply voltage detection control section for controlling the output of the boosted voltage detection control section as recited within claim 3.

Claims 5-13 have been withdrawn from consideration with respect to the elected species.

Prior Art

The other prior art references cited on the accompanying PTO-892 are deemed relevant to at least some of the claimed inventions. Chow and Oh et al. both show/disclose examples of booster circuits utilizing detection circuits for controlling the clock signals applied to a boosting section. However, each reference shows/discloses a different manner of control. Boosted voltage detector 18 of Oh et al.'s Fig. 1 detects boosted voltage VPP, and if VPP has exceeded a preset level, the detection signal from detector 18 disables clock generator 12 (e.g. see column 2, lines 24-27). Therefore, it is understood that if VPP is less than, or equal to, the given voltage value, the detection signal would allow the clock generator to output its clock signal, thus providing one type of clock control (i.e. on/off). Fig. 5 of Chow shows a booster circuit, wherein boosted voltage detector 33,34 detects boosted voltage VPP, and provides detection signal Vfb, which controls the amplitude of the clock signals provided by clock generator 31 (e.g. see the last half of the patent's abstract), providing another type of clock control (i.e. amplitude). Therefore, these references should also be carefully reviewed and considered, along with the references cited within the formal rejections described previously.

The prior art reference cited on the IDS submitted Feb 23, 2004 was reviewed and considered. It does not show the plurality of boosting capacitors connected in parallel as recited within independent claim 1.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE

Terry L. Englund

17 Aug 2005

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